

LATERAL DMOS TRANSISTORS INCLUDING RETROGRADE REGIONS THEREIN AND METHODS OF FABRICATING THE SAME

CROSS-REFERENCE TO RELATED PATENT APPLICATION

[0001] This application claims priority from Korean Patent Application No. 10-2005-0100892, filed on Oct. 25, 2005, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to semiconductor devices, and more particularly, to Metal Oxide Semiconductor (MOS) devices and methods of fabricating the same.

BACKGROUND OF THE INVENTION

[0003] High-power MOS Field Effect Transistors (hereinafter referred to as "MOSFETs") may have a relatively high input impedance as compared with bipolar transistors, which may result in a relatively high power gain. Furthermore, as MOSFETs may be unipolar devices, they may have little time delay due to accumulation and/or reunion of minority carriers when the devices are turned off. Accordingly, MOSFETs may be widely used in switching mode power supplies, lamp ballasts, and/or motor driving circuits. A Double Diffused MOSFET structure formed using planar diffusion techniques may be used to provide such high power MOSFETs. For example, U.S. Pat. Nos. 5,059,547 and 5,378,912 disclose structures of conventional Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS) transistors.

[0004] FIG. 1 is a cross-sectional view illustrating a conventional LDMOS transistor on a Semiconductor On Insulator (SOI) substrate. Referring now to FIG. 1, a buried oxide layer 103 (for use as a buried insulating layer) is formed on an upper surface of a P-type semiconductor substrate 101. An N-type drift region 105 and a P-type body region 107 are formed on an upper surface of the buried oxide layer 103 to provide an active region. A drain region 109 doped with N⁺ type impurity ions is formed in the N-type drift region 105, and a source region 113 doped with N⁺ type impurity ions is formed in the P-type body region 107. A P⁺ type source contact region 111 is formed adjacent to the source region 113. Also, a gate electrode 115 is formed on the semiconductor substrate 101 on a gate insulating layer 117. A field insulating layer 119, which may be used to improve device breakdown voltage, is formed on a surface of the drift region 105. A channel region may be formed at a surface portion of the body region 107 between the source region 113 and a contact surface where the body region 107 meets the drift region 105 upon application of an appropriate voltage to the gate electrode 115.

[0005] FIG. 2 is a graph illustrating the concentration distribution of the N⁺ type impurity ions implanted in the drift region 105 of the conventional LDMOS transistor illustrated in FIG. 1.

[0006] Referring again to FIG. 1, the drift region 105 is formed by implanting impurity ions, such as phosphorous ions, into a surface of the semiconductor substrate 101 where the drift region 105 will be formed, and diffusing the

impurity ions at a relatively high temperature for a period of time. This diffusion process may be relatively lengthy, and may allow the phosphorous ions on the surface of the semiconductor substrate 101 to diffuse under the surface into a bulk region. A concentration of the impurity ions may be highest adjacent to the field oxide layer at the surface of the semiconductor substrate 101. As such, the impurity concentration distribution may follow a Gaussian distribution, as shown in FIG. 2.

[0007] Thus, when a sufficient bias voltage is applied to the gate electrode 115 and the drain region 109, the resistance may be relatively low adjacent the surface of the semiconductor substrate 101, but may be relatively high in the bulk region. Accordingly, most of the current may flow between the source 113 and the drain 109 regions through the surface of the semiconductor substrate 101. As such, an electric field may be concentrated around a sidewall of the N⁺ drain region 109. For relatively small amounts of current, this may present relatively few problems. However, for larger amounts of current at the sidewall portions, holes and electrons may be increased due to impact ionization, which may deteriorate the breakdown voltage of the device.

[0008] Accordingly, when a relatively high bias voltage is supplied to the gate electrode 115 to increase saturation current in a conventional LDMOS transistor, the breakdown voltage may be decreased, which may worsen a Safe Operating Area (SOA) characteristic of the device. A length of the drift region 105 may be increased to improve the SOA characteristic; however, this may increase the physical dimensions of the device.

SUMMARY OF THE INVENTION

[0009] Some embodiments of the present invention may provide Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS) transistors that include enhanced current characteristics and/or breakdown characteristics as well as a Safe Operating Area (SOA) characteristics.

[0010] Some embodiments of the present invention may also provide methods of fabricating LDMOS transistors having enhanced current characteristics, breakdown characteristics, and/or SOA characteristics.

[0011] According to some embodiments of the present invention, an LDMOS transistor may include a drift region between a channel region and a drain region formed within a semiconductor substrate. The drift region may have a retrograde region with an impurity ion density greater than that of the surface of the semiconductor substrate.

[0012] A density profile of the impurity ions in the drift region may decrease from the surface of the semiconductor substrate and may increase to have a peak value in the retrograde region. The retrograde region may be formed below a bottom of the drain region in a vertical direction. Also, the retrograde region may extend to the bottom of the drain region in the lateral direction, and a point/location of corresponding the peak impurity concentration in the retrograde region may be located within a range of about 1-3 μm from an upper surface of the semiconductor substrate.

[0013] According to other embodiments of the present invention, an LDMOS transistor may include a semiconductor substrate. A drift region of a first conductivity type formed under an upper surface of the semiconductor sub-